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KEY=SOI - RICHARD CARLEE

Low Power Analog CMOS for Cardiac Pacemakers Design and Optimization in Bulk and SOI Technologies Springer Science & Business Media *Low Power Analog CMOS for Cardiac Pacemakers proposes new techniques for the reduction of power consumption in analog integrated circuits. Our main example is the pacemaker sense channel, which is representative of a broader class of biomedical circuits aimed at qualitatively detecting biological signals. The first and second chapters are a tutorial presentation on implantable medical devices and pacemakers from the circuit designer point of view. This is illustrated by the requirements and solutions applied in our implementation of an industrial IC for pacemakers. There from, the book discusses the means for reduction of power consumption at three levels: base technology, power-oriented analytical synthesis procedures and circuit architecture.* **Rapid Thermal and Other Short-time Processing Technologies II Proceedings of the International Symposium The Electrochemical Society** "*Electronics, Dielectric Science and Technology, and High Temperature Materials Divisions.*" **Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation 16th International Workshop, PATMOS 2006, Montpellier, France, September 13-15, 2006, Proceedings Springer** *This book constitutes the refereed proceedings of the 16th International Workshop on Power and Timing Modeling, Optimization and Simulation, PATMOS 2006. The book presents 41 revised full papers and 23 revised poster papers together with 4 key notes and 3 industrial abstracts. Topical sections include high-level design, power estimation and modeling memory and register files, low-power digital circuits, busses and interconnects, low-power techniques, applications and SoC design, modeling, and more.* **Silicon-on-Insulator Technology: Materials to VLSI Materials to VLSI Springer Science & Business Media** *Silicon-on-Insulator Technology: Materials to VLSI, Third Edition, retraces the evolution of SOI materials, devices and circuits over a period of roughly twenty years. Twenty years of progress, research and development during which SOI material fabrication techniques have been born and abandoned, devices have been invented and forgotten, but, most importantly, twenty years during which SOI Technology has little by little proven it could outperform bulk silicon in every possible way. The turn of the century turned out to be a milestone for the semiconductor industry, as high-quality SOI wafers suddenly became available in large quantities. From then on, it took only a few years to witness the use of SOI technology in a wealth of applications ranging from audio amplifiers and wristwatches to 64-bit microprocessors. This book presents a complete and state-of-the-art review of SOI materials, devices and circuits. SOI fabrication and characterization techniques, SOI CMOS processing, and the physics of the SOI MOSFET receive an in-depth analysis.* **Silicon-on-insulator Technology and Devices XII Proceedings of the International Symposium The Electrochemical Society Silicon-on-Insulator Technology Materials to VLSI Springer Science & Business Media** *Silicon-on-Insulator Technology: Materials to VLSI, 2nd Edition describes the different facets of SOI technology. SOI chips are now commercially available and SOI wafer manufacturers have gone public. SOI has finally made it out of the academic world and is now a big concern for every major semiconductor company. SOI technology has indeed deserved serious recognition: high-temperature (400°C), extremely rad-hard (500 Mrad(Si)), high-density (16 Mb, 0.9-volt DRAM), high-speed (several GHz) and low-voltage (0.5 V) SOI circuits have been demonstrated. Strategic choices in favor of the use of SOI for low-voltage, low-power portable systems have been made by several major semiconductor manufacturers. Silicon-on-Insulator Technology: Materials to VLSI, 2nd Edition presents a complete and state-of-the-art review of SOI materials, devices and circuits. SOI fabrication and characterization techniques, SOI device processing, the physics of the SOI MOSFET as well as that of SOI other devices, and the performances of SOI circuits are discussed in detail. The SOI specialist will find this book invaluable as a source of compiled references covering the different aspects of SOI technology. For the non-specialist, the book serves as an excellent introduction to the topic with detailed, yet simple and clear explanations. Silicon-on-Insulator Technology: Materials to VLSI, 2nd Edition is recommended for use as a textbook for classes on semiconductor device processing and physics. The level of the book is appropriate for teaching at both the undergraduate and graduate levels. Silicon-on-Insulator Technology: Materials to VLSI, 2nd Edition includes the new materials, devices, and circuit concepts which have been devised since the publication of the first edition. The circuit sections, in particular, have been updated to present the performances of SOI devices for low-voltage, low-power applications, as well as for high-temperature, smart-power, and DRAM applications. The other sections, such as those describing SOI materials, the physics of the SOI MOSFET and other devices have been updated to present the state of the art in SOI technology.* **Semiconductor Wafer Bonding VIII : Science, Technology, and Applications Proceedings of the International Symposium The Electrochemical Society Smart Adaptive Systems on Silicon Springer Science & Business Media** *Intelligent/smart systems have become common practice in many engineering applications. On the other hand, current low cost standard CMOS technology (and future foreseeable developments) makes available enormous potentialities. The next breakthrough will be the design and development of "smart adaptive systems on silicon" i.e. very power and highly size efficient complete systems (i.e. sensing, computing and "actuating" actions) with intelligence on board on a single silicon die. Smart adaptive systems on silicon will be able to "adapt" autonomously to the changing environment and will be able to implement "intelligent" behaviour and both perceptual and cognitive tasks. At last, they will communicate through wireless channels, they will be battery supplied or remote powered (via inductive coupling) and they will be ubiquitous in our every day life. Although many books deal with research and engineering topics (i.e. algorithms, technology, implementations, etc.) few of them try to bridge the gap between them and to address the issues related to feasibility, reliability and applications. Smart Adaptive Systems on Silicon, though not exhaustive, tries to fill this gap and to give answers mainly to the feasibility and reliability issues. Smart Adaptive Systems on Silicon mainly focuses on the analog and mixed mode implementation on silicon because this approach is amenable of achieving impressive energy and size efficiency. Moreover, analog systems can be more easily interfaced with sensing and actuating devices.* **Solid State Circuits Technologies BoD – Books on Demand** *The evolution of solid-state circuit technology has a long history within a relatively short period of time. This technology has lead to the modern information society that connects us and tools, a large market, and many types of products and applications. The solid-state circuit technology continuously evolves via breakthroughs and improvements every year. This book is devoted to review and present novel approaches for some of the main issues involved in this exciting and vigorous technology. The book is composed of 22 chapters, written by authors coming from 30 different institutions located in 12 different countries throughout the Americas, Asia and Europe. Thus, reflecting the wide international contribution to the book. The broad range of subjects presented in the book offers a general overview of the main issues in modern solid-state circuit technology. Furthermore, the book offers an in depth analysis on specific subjects for specialists. We believe the book is of great scientific and educational value for many readers. I am profoundly indebted to the support provided by all of those involved in the work. First and foremost I would like to acknowledge and thank the authors who worked hard and generously agreed to share their results and knowledge. Second I would like to express my gratitude to the Intech team that invited me to edit the book and give me their full support and a fruitful experience while working together to combine this book.* **CMOSET 2011 Energy, Radiation, and Wireless Track Presentation Slides CMOS Emerging Technologies Nanoscale MOS Transistors Semi-Classical Transport and Applications Cambridge University Press** *Written from an engineering standpoint, this book provides the theoretical background and physical insight needed to understand new and future developments in the modeling and design of n- and p-MOS nanoscale transistors. A wealth of applications, illustrations and examples connect the methods described to all the latest issues in nanoscale MOSFET design. Key areas covered include: • Transport in arbitrary crystal orientations and strain conditions, and new channel and gate stack materials • All the relevant transport regimes, ranging from low field mobility to quasi-ballistic transport, described using a single modeling framework • Predictive capabilities of device models, discussed with systematic comparisons to experimental results* **Handbook of Semiconductor Manufacturing Technology CRC Press** *Retaining the comprehensive and in-depth approach that cemented the bestselling first edition's place as a standard reference in the field, the Handbook of Semiconductor Manufacturing Technology, Second Edition features new and updated material that keeps it at the vanguard of today's most dynamic and rapidly growing field. Iconic experts Robert Doering and Yoshio Nishi have again assembled a team of the world's leading specialists in every area of semiconductor manufacturing to provide the most reliable, authoritative, and industry-leading information available. Stay Current with the Latest Technologies In addition to updates to nearly every existing chapter, this edition features five entirely new contributions on... Silicon-on-insulator (SOI) materials and devices Supercritical CO2 in semiconductor cleaning Low-κ dielectrics Atomic-layer deposition Damascene copper electroplating Effects of terrestrial radiation on integrated circuits (ICs) Reflecting rapid progress in many areas, several chapters were heavily revised and updated, and in some cases, rewritten to reflect rapid advances in such areas as interconnect technologies, gate dielectrics, photomask fabrication, IC packaging, and 300 mm wafer fabrication. While no book can be up-to-the-minute with the advances in the semiconductor field, the Handbook of Semiconductor Manufacturing Technology keeps the most important data, methods, tools, and techniques close at hand.* **Microelectronics Technology and Devices - SBMicro 2008 The Electrochemical Society** *The SBMicro symposium is a forum dedicated to fabrication and modeling of microsystems, integrated circuits and devices. The goal of the symposium is to bring together researchers in the areas of processing, materials, characterization, modeling and TCAD of integrated circuits, microsensors, microactuators and MEMS. This issue of ECS Transactions contains the papers presented at the 2008 conference.* **Dual Mode Logic A New Paradigm for Digital IC Design Springer Nature** *This book presents Dual Mode Logic (DML), a new design paradigm for digital integrated circuits. DML logic gates can operate in two modes, each optimized for a different metric. Its on-the-fly switching between these operational modes at the gate, block and system levels provide maximal E-D optimization flexibility. Each highly detailed chapter has multiple illustrations showing how the DML paradigm seamlessly implements digital circuits that dissipate less energy while simultaneously improving performance and reducing area without a significant compromise in reliability. All the facets of the DML methodology are covered, starting from basic concepts, through single gate optimization, general module optimization, design trade-offs and new ways DML can be integrated into standard design flows using standard EDA tools. DML logic is compatible with numerous applications but is particularly advantageous for ultra-low power, reliable high performance systems, and advanced scaled technologies Written in language accessible to students and design engineers, each topic is oriented toward immediate application by all those interested in an alternative to CMOS logic. Describes a novel, promising alternative to conventional CMOS logic, known as Dual Mode Logic (DML), with which a single gate can be operated selectively in two modes, each optimized for a different metric (e.g., energy consumption, performance, size); Demonstrates several techniques at the architectural level, which can result in high energy savings and improved system performance; Focuses on the tradeoffs between power, area and speed including optimizations at the transistor and gate level, including alternatives to DML basic cells; Illustrates DML efficiency for a variety of VLSI applications.* **Low-Power CMOS Design John Wiley & Sons** *This collection of important papers provides a comprehensive overview of low-power system design, from component technologies and circuits to architecture, system design, and CAD techniques. LOW POWER CMOS DESIGN summarizes the key low-power contributions through papers written by experts in this evolving field.* **Computational Science - ICCS 2007 7th International Conference, Beijing China, May 27-30, 2007, Proceedings, Part IV Springer** *Part of a four-volume set, this book constitutes the refereed proceedings of the 7th International Conference on Computational Science, ICCS 2007, held in Beijing, China in May 2007. The papers cover a large volume of topics in computational science and related areas, from multiscale physics to wireless networks, and from graph theory to tools for program development.* **ESD Circuits and Devices John Wiley & Sons** "*Electrostatic discharge (ESD)*"--*Page xxi.* **Extreme Environment Electronics CRC Press** *Unfriendly to conventional electronic devices, circuits, and systems, extreme environments represent a serious challenge to designers and mission architects. The first truly comprehensive guide to this specialized field, Extreme Environment Electronics explains the essential aspects of designing and using devices, circuits, and electronic systems intended to operate in extreme environments, including across wide temperature ranges and in radiation-intense scenarios such as space. The Definitive Guide to Extreme Environment Electronics Featuring contributions by some of the world's foremost experts in extreme environment electronics, the book provides in-depth information on a wide array of topics. It begins by describing*

the extreme conditions and then delves into a description of suitable semiconductor technologies and the modeling of devices within those technologies. It also discusses reliability issues and failure mechanisms that readers need to be aware of, as well as best practices for the design of these electronics. Continuing beyond just the "paper design" of building blocks, the book rounds out coverage of the design realization process with verification techniques and chapters on electronic packaging for extreme environments. The final set of chapters describes actual chip-level designs for applications in energy and space exploration. Requiring only a basic background in electronics, the book combines theoretical and practical aspects in each self-contained chapter. Appendices supply additional background material. With its broad coverage and depth, and the expertise of the contributing authors, this is an invaluable reference for engineers, scientists, and technical managers, as well as researchers and graduate students. A hands-on resource, it explores what is required to successfully operate electronics in the most demanding conditions. **Low-Power CMOS Circuits Technology, Logic Design and CAD Tools CRC Press** *The power consumption of microprocessors is one of the most important challenges of high-performance chips and portable devices. In chapters drawn from Piguet's recently published Low-Power Electronics Design, Low-Power CMOS Circuits: Technology, Logic Design, and CAD Tools addresses the design of low-power circuitry in deep submicron technologies. It provides a focused reference for specialists involved in designing low-power circuitry, from transistors to logic gates. The book is organized into three broad sections for convenient access. The first examines the history of low-power electronics along with a look at emerging and possible future technologies. It also considers other technologies, such as nanotechnologies and optical chips, that may be useful in designing integrated circuits. The second part explains the techniques used to reduce power consumption at low levels. These include clock gating, leakage reduction, interconnecting and communication on chips, and adiabatic circuits. The final section discusses various CAD tools for designing low-power circuits. This section includes three chapters that demonstrate the tools and low-power design issues at three major companies that produce logic synthesizers. Providing detailed examinations contributed by leading experts, Low-Power CMOS Circuits: Technology, Logic Design, and CAD Tools supplies authoritative information on how to design and model for high performance with low power consumption in modern integrated circuits. It is a must-read for anyone designing modern computers or embedded systems.* **Low-Power Electronics Design CRC Press** *The power consumption of integrated circuits is one of the most problematic considerations affecting the design of high-performance chips and portable devices. The study of power-saving design methodologies now must also include subjects such as systems on chips, embedded software, and the future of microelectronics. Low-Power Electronics Design covers all major aspects of low-power design of ICs in deep submicron technologies and addresses emerging topics related to future design. This volume explores, in individual chapters written by expert authors, the many low-power techniques born during the past decade. It also discusses the many different domains and disciplines that impact power consumption, including processors, complex circuits, software, CAD tools, and energy sources and management. The authors delve into what many specialists predict about the future by presenting techniques that are promising but are not yet reality. They investigate nanotechnologies, optical circuits, ad hoc networks, e-textiles, as well as human powered sources of energy. Low-Power Electronics Design delivers a complete picture of today's methods for reducing power, and also illustrates the advances in chip design that may be commonplace 10 or 15 years from now.* **CMOSET 2014 Vol. 4: Optoelectronics and Microelectronics Track CMOS Emerging Technologies Research** *Presentation slides from the Plenary track at the 2014 CMOS Emerging Technologies Research conference in Grenoble, France.* **Electrical Characterization of Silicon-on-Insulator Materials and Devices Springer Science & Business Media** *Silicon on Insulator is more than a technology, more than a job, and more than a venture in microelectronics; it is something different and refreshing in device physics. This book recalls the activity and enthu siasm of our SOI groups. Many contributing students have since then disappeared from the SOI horizon. Some of them believed that SOI was the great love of their scientific lives; others just considered SOI as a fantastic LEGO game for adults. We thank them all for kindly letting us imagine that we were guiding them. This book was very necessary to many people. SOI engineers will certainly be happy: indeed, if the performance of their SOI components is not always outstanding, they can now safely incriminate the relations given in the book rather than their process. Martine, Gunter, and Y. S. Chang can contemplate at last the amount of work they did with the figures. Our SOI accomplices already know how much we borrowed from their expertise and would find it indecent to have their detailed contri butions listed. Jean-Pierre and Dimitris incited the book, while sharing their experience in the reliability of floating bodies. Our families and friends now realize the SOI capability of dielectrically isolating us for about two years in a BOX. Our kids encouraged us to start writing. Our wives definitely gave us the courage to stop writing. They had a hard time fighting the symptoms of a rapidly developing SOI allergy.* **Intelligent Communication, Control and Devices Proceedings of ICICCD 2017 Springer** *The book focuses on the integration of intelligent communication systems, control systems, and devices related to all aspects of engineering and sciences. It contains high-quality research papers presented at the 2nd international conference, ICICCD 2017, organized by the Department of Electronics, Instrumentation and Control Engineering of University of Petroleum and Energy Studies, Dehradun on 15 and 16 April, 2017. The volume broadly covers recent advances of intelligent communication, intelligent control and intelligent devices. The work presented in this book is original research work, findings and practical development experiences of researchers, academicians, scientists and industrial practitioners.* **SOI Lubistors Lateral, Unidirectional, Bipolar-type Insulated-gate Transistors John Wiley & Sons** *Advanced level consolidation of the technology, physicsand design aspects of silicon-on-insulator (SOI)lubistors No comprehensive description of the physics and possibleapplications of the Lubistor can be found in a single source eventhough the Lubistor is already being used in SOI LSIs. The bookprovides, for the first time, a comprehensive understanding of thephysics of the Lubistor. The author argues that a clearunderstanding of the fundamental physics of the pn junction isessential to allowing scientists and engineers to propose newdevices. Since 2001 IBM has been applying the Lubistor tocommercial SOI LSIs (large scale integrated devices) used in PCsand game machines. It is a key device in that it provideselectrostatic protection to the LSIs. The book explains thedevice modeling for such applications, and covers the recent analogcircuit application of the voltage reference circuit. The author also reviews the physics and the modeling of idealand non-ideal pn junctions through reconsideration of theShockley's theory, offering readers an opportunity to studythe physics of pn junction. Pn-junction devices are alreadyapplied to the optical communication system as the light emitterand the receiver. Alternatively, optical signal modulatorsare proposed for coupling the Si optical waveguide with thepn-junction injector. The book also explores the photoniccrystal physics and device applications of the Lubistor. Advanced level consolidation of the technology, physics anddesign aspects of silicon-on-insulator (SOI) lubistors Written by the inventor of the Lubistor, this volume describesthe technology for readers to understand the physics andapplications of the device First book devoted to the Lubistor transistor, presently beingutilized in electrostatic discharge (ESD) applications in SOItechnology, a growing market for semiconductor devices and advancedtechnologies Approaches the topic in a systematic manner, from physicaltheory, through to modelling, and finally circuit applications This is an advanced level book requiring knowledge of electricaland electronics engineering at graduate level. Contents includes: Concept of Ideal pn Junction/Proposalof Lateral, Unidirectional, Bipolar-Type Insulated-Gate Transistor(Lubistor)/ Noise Characteristics and Modeling of Lubistor/NegativeConductance Properties in Extremely Thin SOI Lubistors/ Two-Dimensionally Confined Injection Phenomena at LowTemperatures in Sub-10-nm-Thick SOI Lubistors/ Experimental Studyof Two-Dimensional Confinement Effects on Reverse-Biased CurrentCharacteristics of Ultra-Thin SOI Lubistors/ Gate-Controlled Bipolar Action in Ultra-thin Dynamic ThresholdSOI MOSFET/Sub-Circuit Models of SOI Lubistors for ElectrostaticDischarge Protection Circuit Design and Their Applications/A NewBasic Element for Neural Logic Functions and Functionality inCircuit Applications/Possible Implementation of SOI Lubistors intoConventional Logic Circuits/Potentiality of Electro-Optic ModulatorBased on SOI Waveguide/Principles of ParameterExtraction/Feasibility of Lubistor-Based Avalanche PhotoTransistor* **Device Design and Process Technology for Sub-100 Nm Silicon-on-insulator Metal Oxide Semiconductor Field-effect Transistors Silicon-on-Insulator Technology and Devices 14 The Electrochemical Society** *This issue of ECS Transactions contains papers on silicon-on-insulator subjects including devices, device physics, modelling, simulations, microelectronics, photonics, nano-technology, integrated circuits, radiation hardness, material characterization, reliability, and sensors* **MOSFET Technologies for Double-Pole Four-Throw Radio-Frequency Switch Springer Science & Business Media** *This book provides analysis and discusses the design of various MOSFET technologies which are used for the design of Double-Pole Four-Throw (DP4T) RF switches for next generation communication systems. The authors discuss the design of the (DP4T) RF switch by using the Double-Gate (DG) MOSFET, as well as the Cylindrical Surrounding double-gate (CSDG) MOSFET. The effect of HFO2 (high dielectric material) in the design of DG MOSFET and CSDG MOSFET is also explored. Coverage includes comparison of Single-gate MOSFET and Double-gate MOSFET switching parameters, as well as testing of MOSFETs parameters using image acquisition.* **Fabrication of SiGe HBT BiCMOS Technology CRC Press** *SiGe HBT BiCMOS technology is the obvious groundbreaker of the Si heterostructures application space. To date virtually every major player in the communications electronics market either has SiGe up and running in-house or is using someone else's SiGe fab as foundry for their designers. Key to this success lies in successful integration of the SiGe HBT and Si CMOS, with no loss of performance from either device. Filled with contributions from leading experts, Fabrication of SiGe HBT BiCMOS Technologies brings together a complete discussion of these topics into a single resource. Drawn from the comprehensive and well-reviewed Silicon Heterostructure Handbook, this volume examines the design, fabrication, and application of silicon heterostructure transistors. A novel aspect of this book the inclusion of numerous snapshot views of the industrial state-of-the-art for SiGe HBT BiCMOS technology. It has been carefully designed to provide a useful basis of comparison for the current status and future course of the global industry. In addition to the copious technical material and the numerous references contained in each chapter, the book includes easy-to-reference appendices on the properties of Si and Ge, the generalized Moll-Ross relations, integral charge-control relations, and sample SiGe HBT compact model parameters.* **EDA for IC Implementation, Circuit Design, and Process Technology CRC Press** *Presenting a comprehensive overview of the design automation algorithms, tools, and methodologies used to design integrated circuits, the Electronic Design Automation for Integrated Circuits Handbook is available in two volumes. The second volume, EDA for IC Implementation, Circuit Design, and Process Technology, thoroughly examines real-time logic to GDSII (a file format used to transfer data of semiconductor physical layout), analog/mixed signal design, physical verification, and technology CAD (TCAD). Chapters contributed by leading experts authoritatively discuss design for manufacturability at the nanoscale, power supply network design and analysis, design modeling, and much more. Save on the complete set.* **CMOS RF Modeling, Characterization and Applications World Scientific** *CMOS technology has now reached a state of evolution, in terms of both frequency and noise, where it is becoming a serious contender for radio frequency (RF) applications in the GHz range. Cutoff frequencies of about 50 GHz have been reported for 0.18 æm CMOS technology, and are expected to reach about 100 GHz when the feature size shrinks to 100 nm within a few years. This translates into CMOS circuit operating frequencies well into the GHz range, which covers the frequency range of many of today's popular wireless products, such as cell phones, GPS (Global Positioning System) and Bluetooth. Of course, the great interest in RF CMOS comes from the obvious advantages of CMOS technology in terms of production cost, high-level integration, and the ability to combine digital, analog and RF circuits on the same chip. This book discusses many of the challenges facing the CMOS RF circuit designer in terms of device modeling and characterization, which are crucial issues in circuit simulation and design.* **Silicon-on-insulator Technology and Devices XI Proceedings of the International Symposium The Electrochemical Society Power Management for Internet of Everything CRC Press** *In this book, several advanced topics in the area of Power Management Analog and Mixed-Signal Circuits and Systems have been addressed. The fundamental aspects of these topics are discussed, and state-of-the-art developments are presented. The book covers subject areas like bio-sensors co-integration with nanotechnology, and for these CMOS circuits one popular application could be personalized medicine. Having seen the power assets for such technologies, and knowing what challenges these present for the circuits and systems designer, remote powering and sensors solutions are reviewed in the second chapter. The third chapter contains an industrial contribution on remote powering, presenting energy harvesting from the RF field to power a target wireless sensor network consumption. Having touched the idea of the low current consumption, μA or Nano-Amp range and their transient behaviours are also described. Digital and large-scale integrated circuits - seen from an academic point of view - is included in chapter five, and this same topic from an industrial point of view is given in the chapter thereafter. An additional topic on the hall sensor, applied in an automotive case study, is then also presented. Approaching the duty-cycling of active mode, oscillator for timers and system-level power management including the cloud are covered in the last chapters. Power Management for Internet of Everything targets post-graduate students and those persons active in industry, whom understand and can connect system design with system on chip (SoC) and mixed-signal design as broader set of circuits and systems. The topic of Internet of Things (IoT), ranging from data converters for sensor interfaces to radios and software application, is also addressed from the viewpoint of power and energy management. The contents ensures a good balance between academia and industry, combined with a judicious selection of distinguished international authors.* **Electrostatic Discharge Protection Advances and Applications CRC Press** *Electrostatic discharge (ESD) is one of the most prevalent threats to electronic components. In an ESD event, a finite amount of charge is transferred from one object (i.e., human body) to another (i.e., microchip). This process can result in a very high current passing through the microchip within a very short period of time. Thus, more than 35 percent of single-event chip damages can be attributed to ESD events, and designing ESD structures to protect integrated circuits against the ESD stresses is a high priority in the semiconductor industry. Electrostatic Discharge Protection: Advances and Applications delivers timely coverage of component- and system-level ESD protection for semiconductor devices and integrated circuits. Bringing together contributions from internationally respected researchers and engineers with expertise in ESD design, optimization, modeling, simulation, and characterization, this book bridges the gap between theory and practice to offer valuable insight into the state of the art of ESD protection. Amply illustrated with tables, figures, and case studies, the text: Instills a deeper understanding of ESD events and ESD protection design principles Examines vital processes including Si CMOS, Si BCD, Si SOI, and GaN technologies Addresses important aspects pertinent to the modeling and simulation of ESD protection solutions Electrostatic Discharge Protection: Advances and Applications provides a single source for cutting-edge information vital to the research and development of effective, robust ESD protection solutions for semiconductor devices and*

integrated circuits. **Encyclopedia of Computer Science and Technology Volume 36 - Supplement 21: Artificial Intelligence in Economics and Management to Requirements Engineering CRC Press** *Artificial Intelligence in Economics and Managemetn to Requirements Engineering* **CMOS Technology Optimization for Low Voltage, Low Power Applications ESD Design Challenges and Strategies in Deeply-scaled Integrated Circuits Stanford University** *It is the main objective of this work to address the scaling and design challenges of ESD protection in deeply scaled technologies. First, the thesis introduces the on-chip ESD events, the scaling and design challenges, and the nomenclatures necessary for later chapters. The ESD design window and the I/O schematics for both rail clamping and local clamping ESD schemes are illustrated. Then, the thesis delves into the investigation of the input and output driver devices and examines their robustness under ESD. The input driver's oxide breakdown levels are evaluated in deeply scaled technologies. The output driver's trigger and breakdown voltages are improved appreciably by applying circuit and device design techniques. The ESD device sections first discuss rail-based clamping, a widely used protection scheme. Two diode-based devices, namely the gated diode and substrate diode, are investigated in detail with SOI test structures. Characterization is based on DC current-voltage (I-V), Very Fast Transmission Line Pulse (VF-TLP), capacitance, and leakage measurements. Improvements in performance are realized. Technology computer aided design (TCAD) simulations help understand the physical effects and design tradeoffs. Then, the following section focuses on the local clamping scheme. Two devices, the field-effect diode (FED) and the double-well FED (DWFED), are developed and optimized in an SOI technology. Trigger circuits are designed to improve the turn-on speed. The advantages of local clamping is highlighted and compared with the rail-based clamping. The results show that the FED is a suitable option for power clamping applications and the DWFED is most suitable for pad-based local clamping. The thesis presents an ESD protection design methodology, which takes advantage of the results and techniques from pervious chapters and put each element into a useful format. Based on the correlation of package level and in-lab test results, a design process based on CDM target definition and device optimization, discharge path analysis, parasitic minimization, I/O data rate estimation and finally ESD and performance characterization is used sequentially to systematically realize the overall design goals.* **Interlayer Dielectrics for Semiconductor Technologies Elsevier** *Semiconductor technologies are moving at such a fast pace that new materials are needed in all types of application. Manipulating the materials and their properties at atomic dimensions has become a must. This book presents the case of interlayer dielectrics materials whilst considering these challenges. Interlayer Dielectrics for Semiconductor Technologies cover the science, properties and applications of dielectrics, their preparation, patterning, reliability and characterisation, followed by the discussion of different materials including those with high dielctric constants and those useful for waveguide applications in optical communications on the chip and the package. * Brings together for the FIRST time the science and technology of interlayer deilectrics materials, in one volume * written by renowned experts in the field * Provides an up-to-date starting point in this young research field.* **VLSI Science and Technology/1984 Materials for High Speed/high Density Applications : Proceedings of the Second International Symposium on Very Large Scale Integration Science and Technology Photonics and Electronics with Germanium John Wiley & Sons** *Representing a further step towards enabling the convergence of computing and communication, this handbook and reference treats germanium electronics and optics on an equal footing. Renowned experts paint the big picture, combining both introductory material and the latest results. The first part of the book introduces readers to the fundamental properties of germanium, such as band offsets, impurities, defects and surface structures, which determine the performance of germanium-based devices in conjunction with conventional silicon technology. The second part covers methods of preparing and processing germanium structures, including chemical and physical vapor deposition, condensation approaches and chemical etching. The third and largest part gives a broad overview of the applications of integrated germanium technology: waveguides, photodetectors, modulators, ring resonators, transistors and, prominently, light-emitting devices. An invaluable one-stop resource for both researchers and developers.* **The ESD Handbook John Wiley & Sons** *A practical and comprehensive reference that explores Electrostatic Discharge (ESD) in semiconductor components and electronic systems The ESD Handbook offers a comprehensive reference that explores topics relevant to ESD design in semiconductor components and explores ESD in various systems. Electrostatic discharge is a common problem in the semiconductor environment and this reference fills a gap in the literature by discussing ESD protection. Written by a noted expert on the topic, the text offers a topic-by-topic reference that includes illustrative figures, discussions, and drawings. The handbook covers a wide-range of topics including ESD in manufacturing (garments, wrist straps, and shoes); ESD Testing; ESD device physics; ESD semiconductor process effects; ESD failure mechanisms; ESD circuits in different technologies (CMOS, Bipolar, etc.); ESD circuit types (Pin, Power, Pin-to-Pin, etc.); and much more. In addition, the text includes a glossary, index, tables, illustrations, and a variety of case studies. Contains a well-organized reference that provides a quick review on a range of ESD topics Fills the gap in the current literature by providing information from purely scientific and physical aspects to practical applications Offers information in clear and accessible terms Written by the accomplished author of the popular ESD book series Written for technicians, operators, engineers, circuit designers, and failure analysis engineers, The ESD Handbook contains an accessible reference to ESD design and ESD systems.*